REMARKS

Claims 1-19 are pending in the present application. The applicants respectfully request reconsideration and allowance of the present application in view of the above amendments and the following remarks.

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all certified copies of the priority documents have been received.

The applicants acknowledge and appreciate receiving a copy of the form PTO-1449 submitted with the Information Disclosure Statement filed on December 20, 2001 on which the Examiner has initialed all listed items.

The disclosure is objected to because of informalities. The specification is amended herein to address the noted informalities.

Claims 3 stands rejected under 35 USC §112, second paragraph, as being allegedly indefinite. While the propriety of the rejection is questioned, the claim is amended herein to improve the clarity thereof with regard to the noted elements, e.g. "the monitor" and "the predetermined input terminal".

To support a proper rejection under 35 USC §112, second paragraph and establish a *prima facie* case of indefiniteness, the Examiner must provide evidence that one of ordinary skill in the art would not have been able to determine *with a reasonable degree of certainty*, the scope of the claims. No such evidence has been provided and thus a *prima facie* case has not properly been established. However, to improve clarity, proper antecedent basis for the terms "the monitor" and "the predetermined input terminal" is provided in connection with additional amendments set forth in the present response, and not for reasons related to the rejection herein above under 35 USC §112, second paragraph.

Claims 1-19 stand rejected under 35 USC §102(e) as being allegedly anticipated by Tetsushi, U.S. Patent No. 6,198,820. Independent claims 1, 3, and 15 are amended herein to further distinguish over Tetsushi.

Claim 1, as amended, recites an intermittent time measuring means which operates to measure an intermittent time which is a substantial pause period of the CPU. The CPU is configured to read the intermittent time measured by the intermittent time measuring means, measure, using its own software process, an operation time in which the CPU is in the operating condition, and measure a total time from a start time of the intermittent operation of the CPU by accumulating the intermittent time and the operation time. In accordance with the claimed invention, the CPU can more precisely measure a very long period such as, for example, several tens of hours or several days and can reduce power consumption thereby.

In contrast, Tetsushi at best, measures only the intermittent time but not in the manner of the claimed invention. Tetsushi repeatedly counts a slot counter up to a prescribed value however fails to disclose the claimed intermittent time measuring means. As noted, for example, on page 8, line 16 and 17, the intermittent time measuring means includes timer block 17 and in the paragraph beginning on page 10, line 23, timer block 17 is shown to form a measured value Ta in a format which may be read by the CPU 3. Tetsushi fails to show the formation of a measured value and further fails to disclose a CPU configured to measure, using its own software process, an operation time in which the CPU is in the operating condition, and to measure a total time from a start time of the intermittent operation of the CPU by accumulating the intermittent time and the operation time.

Claim 3, as amended, recites, *inter alia*, a level detecting circuit reading and determining, when the CPU is in the stop condition, a level of a monitor object signal supplied to a

predetermined input terminal of the microcomputer in every constant period and then raising the CPU to the operating condition from the stop condition when the determined level reaches a particular level, and an automatic signal reading means for reading and determining, when the CPU is in the stop condition, a level of the monitor object signal supplied to the predetermined input terminal of the microcomputer in every constant period and then raising the CPU to the operating condition from the stop condition when the determined level reaches the particular level.

Tetsushi fails to disclose the claimed level detecting circuit, and correspondingly fails to disclose the claimed automatic signal reading means for reading and determining, when the CPU is in the stop condition, a level of the monitor object signal. In support of the rejection, col 9 lines 1-19, 39-44; col 9 line 66 – col 10, line 21 is cited as allegedly disclosing the claimed automatic signal reading mean including reading and determining a level of the monitor object signal. Applicants respectfully disagree and request that the Examiner point out with specificity which feature of Tetsushi is alleged to amount to, for example, the portion of Tetsushi that discloses the automatic signal reading mean including reading and determining a level of the monitor object signal, particularly given that Applicants contend that Tetsushi fails to disclose the claimed level detecting circuit.

Claim 15, as amended, recites, *inter alia*, a timer interlocking control means receiving the sub-clock to operate, and for outputting the drive signal to the external apparatus depending on the predetermined setting time. In support of the rejection, col 8, lines 55-56, col 9, line 1, col 12 line 19 are cited.

In the cited section, Tetsushi shows, at best, an intermittent control section associated with the portable remote terminal. It should be noted however that Tetsushi fails to show a timer

interlocking control means receiving the sub-clock to operate, and for outputting the drive signal to the external apparatus depending on the predetermined setting time. A close review of Fig. 7 of Tetsushi reveals no connection to an external device. Fig. 3 of Tetsushi shows an external interface 3b, however this interface is for transfer of data (col 7, line 37) and does not amount to the claimed features as noted above, where a drive signal is output to an external apparatus depending on the predetermined setting time.

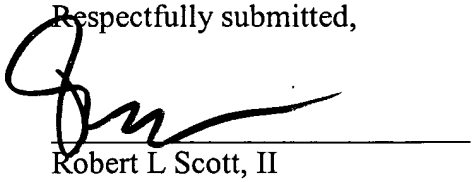
Accordingly, for at least the reasons set forth hereinabove, a *prima facie* case of anticipation has not properly been established in that the applied reference fails to disclose all the claimed features as required. It is respectfully requested that the rejection of independent claims 1, 3, and 15 be reconsidered and withdrawn.

Claims 2, 4-14, and 16-19, by virtue of depending from independent claims 1, 3, and 15, are allowable for at least the reasons set forth hereinabove. It is respectfully requested therefore that the rejection of claims 2, 4-14, and 16-19 be reconsidered and withdrawn.

In view of the foregoing, the applicants respectfully submit that the present application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

Please charge any unforeseen fees that may be due to Deposit Account No. 50-1147.

Respectfully submitted,



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